Reg. No. :

Question Paper Code : X 67572

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Sixth Semester
Electronics and Communication Engineering
EC 1354 – VLSI DESIGN
(Common to Electrical and Electronics Engineering)
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Prepare a comparison table between nMOS and pMOS.
2. Define threshold voltage.
3. Give the expression for inductance of a conductor on a chip.
4. Define delay time.
5. Draw the transfer characteristics of a CMOS inverter.
6. How do you overcome short channel effects in MOS transistors ?
7. What are the various objectives of placement in the physical design process ?
8. List the methods of CMOS testing.
9. Define FSM.
10. What are gate primitives ?

PART – B **(5×16=80 Marks)**

11. a) Discuss in detail about second order effects of MOS transistor. **(16)**

(OR)

b) Explain in detail about basic CMOS technology. **(16)**

12. a) Design a CMOS and Dynamic CMOS circuits that implements the function f = c.k.r + r.k.p + g.m. Assess the efficiency of each schemes and compare their performances.

(OR)

b) Design a 16:1 Multiplexer using :

i) CMOS and

ii) Transmission Gates assess the efficiency of each implementation.

13. a) i) Explain in detail about the scaling concept and design margin concepts. **(12)**

ii) Write short notes about the transistor sizing for the performance in combinational Networks. **(4)**

(OR)

b) Describe in detail about the resistance and capacitance estimation calculation in a CMOS circuit with the proper loads and drivers. **(16)**

14. a) i) Design a generic carry look ahead adder. **(10)**

ii) Brief on high speed adder circuits. **(6)**

(OR)

b) i) Design a circuit for a 4 bit unsigned magnitude comparator and explain. **(8)**

ii) Describe about delay modeling and clock distribution in ICs. **(8)**

15. a) Explain the following with an example :

i) Tasks and functions **(4)**

ii) Test bench for 4 : 1 multiplexer **(4)**

iii) Difference between always and initial **(4)**

iv) Blocking and non-blocking statements. **(4)**

(OR)

b) i) Design and develop a project in HDL to compare x5 x4 x3 x2 x1 x0 with y5 y4 y3 y2 y1 y0. Check the output by means of test bench. **(10)**

ii) Give the different types of operators in Verilog HDL and explain any three. **(6)**